DOUBLE DATA RATE SYNCHRONOUS SRAM WITH 100% BUS UTILIZATION

Stanley A. Hronik

ABSTRACT OF THE INVENTION

A synchronous memory circuit is capable of double data transfer rate per clock cycle, 100% bus utilization (i.e., no idle clock cycles in bus turn arounds), and has only one clock cycle of latency in each of read and write burst operations. The memory circuit has a data bus 202, at least two memory blocks (20, 30), a multiplexer (120) for receiving two read data items from respective two memory blocks in a read burst operation and allowing one of the two read data items to be provided on the data bus half a clock cycle after the read burst operation is initiated and allowing the other one of the two read data items to be provided on the data bus one clock cycle after the read burst operation is initiated, and two registers (50, 70) for storing respective two write data items provided on the data bus in a first write burst operation wherein one of the two write data items is written to one of the two memory blocks at the initiation of a next write burst operation following the first write burst operation and the other one of the two write data items is written to the other one of the two memory blocks half a clock cycle after the initiation of the next write burst operation, wherein in two consecutive clock cycles the two write data items are capable of being transferred to the memory circuit via the data bus and the two read data items are capable of being transferred from the memory circuit via the data bus.